What is claimed is:

1. A memory device comprising:

a read only memory (ROM) cell hard programmed to a first data state;

a dynamic memory cell; and

access circuitry to couple the ROM cell and the dynamic memory cell to differential digit lines.

2. The memory device of claim 1 wherein the access circuitry comprises:

a first transistor coupled between the ROM cell and a first digit line; and

a second transistor coupled between the dynamic memory cell and a second digit line, wherein gate connections of the first and second transistors are coupled to different word lines.

3. The memory device of claim 1 wherein the ROM cell is hard programmed to Vcc.

4. The memory device of claim 1 wherein the ROM cell is hard programmed to Vss.

5. The memory device of claim 1 wherein the ROM cell is a capacitor cell hard programmed using an electrical potential to short a dielectric layer of the ROM cell.

6. The memory device of claim 1 wherein the ROM cell is a capacitor cell hard programmed with a physical conductor fabricated between capacitor plates of the ROM cell.

7. The memory device of claim 1 wherein the ROM cell is a capacitor cell hard programmed by providing a high leakage path from a storage node of the ROM cell.

8. The memory device of claim 1 wherein the ROM cell is a capacitor cell hard programmed by physically shorting a storage node of the ROM cell to receive a voltage signal.

9. A half-density read only memory (ROM) embedded dynamic random access memory (DRAM) device comprising:

a DRAM array comprising first dynamic memory cells;

a ROM array comprising hard programmed non-volatile memory cells and second dynamic memory cells;

sense amplifier circuitry coupled to differential digit lines of the ROM array;

word lines to access rows of the memory ROM array; and

access circuitry to couple one of the non-volatile memory cells and one of the second dynamic memory cells to the differential digit lines in response to a pair of word line signals.

10. The ROM embedded DRAM device of claim 9 wherein the access circuitry comprises:

a first transistor coupled between the non-volatile memory cells and a first digit line; and

a second transistor coupled between the second dynamic memory cells and a second digit line, wherein gate connections of the first and second transistors are coupled to receive first and second word line signals, respectively.

11. The ROM embedded DRAM device of claim 9 wherein the non-volatile memory cells are hard programmed to Vcc and the second dynamic memory cells are not programmed.

12. The ROM embedded DRAM device of claim 9 wherein the non-volatile memory cells are hard programmed to Vss and the second dynamic memory cells are not programmed.

13. The memory device of claim 9 wherein the ROM cell is a capacitor cell hard programmed,

using an electrical potential to short a dielectric layer of the ROM cell,

using a physical conductor fabricated between capacitor plates of the ROM cell,

using a high leakage path from a storage node of the ROM cell, or

using a physical short between a storage node of the ROM cell to receive a voltage signal.

14. A half-density read only memory (ROM) comprising:

an array of ROM cells each comprising first and second memory cells, the first memory cell is programmed in a non-volatile manner to a first voltage and the second memory cell is a volatile memory cell capacitor; and

access circuitry coupled to read each ROM cell, wherein the access circuitry electrically couples the first and second memory cells to differential sensing circuitry.

15. The half-density ROM of claim 14 wherein the first voltage has a level of Vcc.

16. The half-density ROM of claim 14 wherein the first voltage has a level of Vss.

17. A method of operating a read-only memory comprising:

programming a first memory cell in a non-volatile manner to a first data state;

providing an un-programmed volatile memory cell; and

accessing both the first and second memory cell capacitors in response to word line signals.

18. The method of claim 17 wherein the first memory cell is a capacitor having first and second plates permanently coupled together.

19. The method of claim 18 wherein the first and second capacitor plates are permanently coupled by applying a potential sufficient to break down an intermediate dielectric layer of the first memory cell capacitor.

20. The method of claim 18 wherein the first and second capacitor plates are permanently coupled by fabricating a conductor between the first and second capacitor plates.

21. The method of claim 17 wherein the first memory cell comprises a plate electrically coupled to a bias voltage.

22. The method of claim 21 wherein the plate is electrically coupled to a bias voltage equal to Vcc or Vss.